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09/879,637	06/12/2001	Chang-Whan Jung	SAM-210	4260

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EXAMINER

NGUYEN, MINH T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



AK

**Office Action Summary**

Applicant(s)

09/879,637

Applicant(s)

JUNG ET AL.

Examiner

Minh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 July 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                      6) ☐ Other: \_\_\_\_\_



## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/2/03 has been entered.

### ***Claim Objections***

2. Claim 6 is objected to because of the following informalities: "the power supply voltage" recited on line 1 should be changed to -- a power supply voltage -- to avoid potential antecedent basis problem. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No.

'391, issued to Haraguchi.



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As per claim 1, Haraguchi discloses a fuse circuit (Fig. 17) for a semiconductor integrated circuit, comprising:

a plurality of fuses (163 and 263); and

a plurality of transmission circuits (TG14 and TG24), each transmission circuit being coupled to a corresponding fuse of the plurality of fuses (as shown, TG14 to 163 and TG24 to 263); each transmission circuit for transferring signals from an input node (this is a function of a transmission gate) to an output node in response to a status of the corresponding fuse (depending on whether the corresponding fuse is blown or not, see column 5, lines 52-67), the input and output nodes of respective adjacent transmission circuits being coupled such that the transmission circuits are arranged in series (as shown, TG14 and TG24 are in series).

As per claim 2, met since it is merely an operation of the circuit, i.e., when X1.X2 is selected, the fuses have identical status.

As per claim 3, the first terminal of fuse 163 is connected to the first power supply which is GND and the second terminal of fuse 163 is connected to node 160.

As per claim 4, as shown, the transmission gate TG14 is connected as recited, the primary control terminal connected to node 167 and the secondary control terminal connected to the output of inverter 166; and the recited inverter 166 connected as recited.

As per claim 5, as shown TG14 includes PMOS and NMOS transistors connected as recited.

As per claim 6, the recited power supply voltage reads on the voltage of the signal X1.X2 since the voltage must come from a power supply voltage.



As per claim 7, the recited resistor reads on resistor 162 connected to the second power supply voltage VCC.

As per claim 8, same as claim 1.

As per claim 9, since each of the fuses has two ends, it stores one bit of information, and the information can be anything which includes the information relevant to the semiconductor integrated circuit.

As per claims 10-12, these claims are rejected for the same reasons noted in claims 4, 5 and 7, respectively.

4. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,517,151, issued to Kubota.

As per claim 1, Kubota discloses a fuse circuit (Fig. 6) for a semiconductor integrated circuit, comprising:

a plurality of fuses (there are four fuses); and

a plurality of transmission circuits (there are four, each transmission circuit is a circuit shown as circuit block 21 less the fuse in that circuit block), each transmission circuit being coupled to a corresponding fuse of the plurality of fuses (as shown, each corresponding fuse is in the same circuit block of the transmission circuit); each transmission circuit for transferring signals from an input node (the node on the left side of each of the circuit blocks 21) to an output node (the node on the right side of each of the circuit blocks 21) in response to a status of the corresponding fuse (depending on whether the corresponding fuse is blown or not), the input and output nodes of respective adjacent transmission circuits being coupled such that the



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transmission circuits are arranged in series (connected in series since the output node of one of the transmission circuit is connected to the input of the next transmission circuit).

As per claim 2, met since it is merely an operation of the circuit.

As per claim 3, each of the fuses includes two ends are shown in Fig. 6, and the lower end of each of the fuses in Fig. 6, which is seen as the first terminal, is connected to a power supply voltage.

As per claim 4, Kubota further discloses each of the transmission circuits comprises:

a transmission gate (for example, the transmission gate 24-1) having an input terminal (the terminal connects to node B) coupled to a corresponding input node, an output terminal (the terminal connects to drain of transistor 26-1) coupled to a corresponding output node (through transistor 23-1), and a primary control terminal (the terminal connects to the gate of transistor 26-1 and the second terminal of the corresponding fuse) connected to the second terminal of the corresponding fuse, and a secondary control terminal (the terminal connects to the output of the corresponding inverter); and

an inverter (the inverter connects to the second terminal of the corresponding fuse) having an input terminal connected to the second terminal of the fuse and the primary control terminal, and an output terminal connected to the secondary control terminal (as shown).

As per claim 5, Kubota further discloses the transmission gate includes a first conductive transistor (the left half of the transmission gate 24-1 is an NMOS type transistor) and a second conductive transistor (the right half of the transmission gate 24-1 is a PMOS type transistor), and these transistors are connected as recited.



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As per claim 6, Kubota further discloses a power supply voltage at node 8 is applied to the input terminal of the first transmission gate 24-1 through the transistor connected diode 11' as shown.

As per claim 7, the recited resistor in each of the transmission circuits reads on the resistor which is connected to the second terminal of the corresponding fuse as shown in Fig. 6, and the resistor is connected as recited.

As per claim 8, Kubota discloses a fuse circuit storing information related to a semiconductor integrated circuit (Fig. 6), comprising:

a plurality of fuses (there are four fuses), each has two ends and one end (the lower end, the first terminal) is connected to a power supply voltage, the fuses storing predetermined information relevant to the semiconductor integrated circuit (determined by whether the fuse is blown or not); and

a plurality of transmission circuits (there are four, each block circuit 21 except the fuse, is seen as a transmission circuit) connected to the fuses as recited for transferring an input signal to an output terminal (when the transmission circuit is closed),

wherein the transmission circuits are connected in series (the output terminal of transmission circuit in the first block 21 is connected to the input terminal of transmission circuit in the second block 21, ...).

As per claim 9, since each of the fuses has two ends, it stores one bit of information, and the information can be anything which includes the information relevant to the semiconductor integrated circuit.



As per claims 10-12, these claims are rejected for the same reasons noted in claims 4, 5 and 7, respectively.

***Response to Arguments***

5. Applicants' arguments with regard to the claims have been considered but they are not persuasive.

Regarding the argument that Kubota fails to teach or suggest each transmission circuit transferring signals "from an input node to an output node in response to a status of the corresponding fuse".

The Examiner disagrees.

Consider the first transmission circuit (includes transmission gates 23-1 and 24-1), when *the status of* the fuse is OFF, the transmission gate (23-1 and 24-1) is ON, the input signal at B *in response* to this status (the fuse is OFF), part of the input signal at B flows through the transmission gate and part of the input signal passes to the output,

when *the status of* the fuse is ON, the transmission gate (23-1 and 24-1) is OFF, the input signal at B *in response* to this status (the fuse is ON), all of the input signal at B flows through the transmission gate,

the recited limitation is met.

The Examiner further notes that claims 1 and 8 do not require when the transmission gate is ON, the input signal is transferred to the output and when the transmission gate is OFF, the input signal is blocked from transferring to the output as argued by the Applicants.



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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Minh Nguyen  
Primary Examiner  
Art Unit 2816

MN  
July 24, 2003